WHAT IS CLAIMED IS:

1. A semiconductor device manufacturing method comprising:

forming an island region including a monocrystalline $Si_{1-x-y}Ge_xC_y$ layer ($1 > x > 0$, $1 > y \geqq 0$) and a peripheral region including an amorphous or polycrystalline $Si_{1-x-y}Ge_xC_y$ layer which surrounds the island region on a monocrystalline Si layer on an insulating film;

subjecting the respective $Si_{1-x-y}Ge_xC_y$ layers to heat treatment; and

forming a monocrystalline $Si_{1-z-w}Ge_zC_w$ layer ($1 > z \geqq 0$, $1 > w \geqq 0$), which becomes an device formation region, on the island region after the heat treatment and removal of a surface oxide film.

2. The method according to claim 1, wherein the forming the monocrystalline island region including the $Si_{1-x-y}Ge_xC_y$ and the amorphous or polycrystalline peripheral region includes forming an oxide film on the monocrystalline Si layer on the insulating film excluding a portion corresponding to the element formation region, and then forming an $Si_{1-x-y}Ge_xC_y$ monocrystalline layer on the monocrystalline Si layer and an $Si_{1-x-y}Ge_xC_y$ polycrystalline layer on the oxide film, respectively.

3. The method according to claim 1, wherein the heat treatment is carried out in an atmosphere

containing oxygen.

4. The method according to claim 1, wherein the heat treatment is carried out in an atmosphere containing oxygen, and thereafter the heat treatment is carried out in an atmosphere without oxygen.

5. The method according to claim 1, wherein a temperature of the heat treatment is 1000℃ or more.

6. The method according to claim 1, wherein a temperature of the heat treatment is from 1150 to 1250℃.

7. The method according to claim 1, wherein a size of the island region is smaller than 20 μm^2.

8. The method according to claim 1, wherein a distance between the island regions is at least 0.1 μm.

9. A semiconductor device manufacturing method comprising:

forming a monocrystalline $Si_{1-x-y}Ge_xC_y$ layer ($1 > x > 0$, $1 > y \geqq 0$) on a monocrystalline Si layer on an insulating film;

forming an island-shaped mask layer on the $Si_{1-x-y}Ge_xC_y$ layer;

making a peripheral region amorphous by ion implantation excluding an island region of the $Si_{1-x-y}Ge_xC_y$ layer covered with the island-shaped mask layer;

subjecting the $Si_{1-x-y}Ge_xC_y$ layer to heat

treatment; and

forming a monocrystalline $Si_{1-z-w}Ge_zC_w$ layer ($1 > z \geqq 0$, $1 > w \geqq 0$), which becomes an device formation region, on the island region of the $Si_{1-x-y}Ge_xC_y$ layer after the heat treatment and removal of a surface oxide film.

10. The method according to claim 9, wherein, ion species for the implantation are one of a Si ion, a C ion or a Ge ion or combination thereof.

11. The method according to claim 9, wherein the heat treatment is carried out in an atmosphere containing oxygen.

12. The method according to claim 9, wherein the heat treatment is carried out in an atmosphere containing oxygen, and thereafter the heat treatment is carried out in an atmosphere without oxygen.

13. The method according to claim 9, wherein a temperature of the heat treatment is 1000℃ or more.

14. The method according to claim 9, wherein a temperature of the heat treatment is from 1150 to 1250℃.

15. The method according to claim 9, wherein a size of the island region is smaller than 20 μm^2.

16. The method according to claim 9, wherein a distance between the island regions is at least 0.1 μm.

17. A semiconductor device manufacturing method

comprising:

forming a first region including a monocrystalline $Si_{1-x-y}Ge_xC_y$ layer ($1 > x > 0$, $1 > y \geqq 0$) on a monocrystalline Si layer on an insulating film and a second region including a slit or hole-shaped amorphous or polycrystalline $Si_{1-x-y}Ge_xC_y$ layer in the first region;

subjecting the respective $Si_{1-x-y}Ge_xC_y$ layers to heat treatment; and

forming, a monocrystalline $Si_{1-z-w}Ge_zC_w$ layer ($1 > z \geqq 0$, $1 > w \geqq 0$), which becomes an device formation region, on the first region after the heat treatment and removal of an surface oxide film.

18. The method according to claim 17, wherein a distance between the slits or between the holes is set within 10 μm.

19. The method according to claim 17, wherein a width of the slit or the hole is at least 0.1 μm.

20. The method according to claim 17, wherein the hole has a long and narrow shape.